

SHEET INDEX

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SYMBOL
SERIAL PERIPHERAL INTERFACE B
ELEMENT IDENT
A

TERM. MOD	FUNC.	TERM.	LOC.	TERM. MOD	FUNC.	TERM.	LOC.
10150	I	309	247	8100	#	114	252
INF000	I	215	247	8110	#	103	252
INF010	I	314	247	8120	#	74	252
INF020	I	211	246	8130	#	201	
INF030	I	310	246	8140	#	018	251
INF040	I	116	245	8150	#	002	250
INF050	I	214	255	8160	#	102	250
INF060	I	205	244	8170	#	107	244
INF070	I	304	244	8180	#	118	340
INF080	I	301	244	8190	#	218	340
INF090	I	003	243	8200	#	219	341
INF100	I	010	242	8210	#	318	341
INF110	I	109	242	8220	#	105	246
INF120	I	207	242	8230	#	017	257
INF130	I	307	241	8240	#	115	247
INF140	I	312	241	8250	#	315	347
INF150	I	212	240	8260	#	005	248
INF160	I	203	240	8270	#	201	309
INF170	I	206	243	8280	#	000,119	345
INF180	I	311	240	8290	#	200,319	347
MYRAB	I	213	340				
MYRBA	I	208	341				
MYRBP	I	308	340				
FL1880	I	317	240				
RSET01	I	006	343				
STR181	I	217	347				
B000	#	113	257				
B010	#	014	257				
B020	#	100	254				
B030	#	117	254				
B040	#	014	255				
B050	#	101	255				
B060	#	001	254				
B070	#	104	254				
B080	#	008	253				
B090	#	313	253				

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	CPS-JK6
CONNECTOR ON FRAME	947C 947A
SERIES FOR LATEST CLASS A CHANGE, (ANY HIGHER SERIES IS ACCEPTABLE).	
ACCEPTABLE SERIES	1

RECORD OF CHANGES

ENG. ISS.	PREV. PURN.	STD.	WFR. DISC.	SEE NOTE

NOTES:

- GROUND RETURN
- UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS. CAPACITANCE VALUES ARE IN MICROFARADS. VALUES PRECEDED BY THE SYMBOL - (PLUS) OR - (MINUS) ARE IN VOLTS.

- BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD. TERM.
418P	16	8
41CF	16	7, 8
175H	1, 32	16, 17
KS-2168B L1	14	7
KS-2168B L3	14	7
KS-2168B L4	14	7
KS-2168B L5	14	7
KS-2168B L6	14	7
KS-2168B L1	16	8

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IN

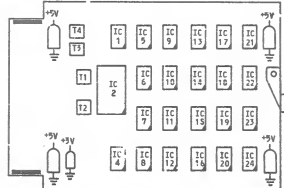
CURRENT DRAIN: 600mA

- BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000, 119
GRD	200, 314

- HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

- INTEGRATED CIRCUIT AND TRANSFORMER LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SHEET INDEX NOTES

- WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
- THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
- THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
- SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
- THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

JK6 CIRCUIT PACK

SERIAL PERIPHERAL INTERFACE B CIRCUIT

AT&T
STANDARD

2

CPS-JK6

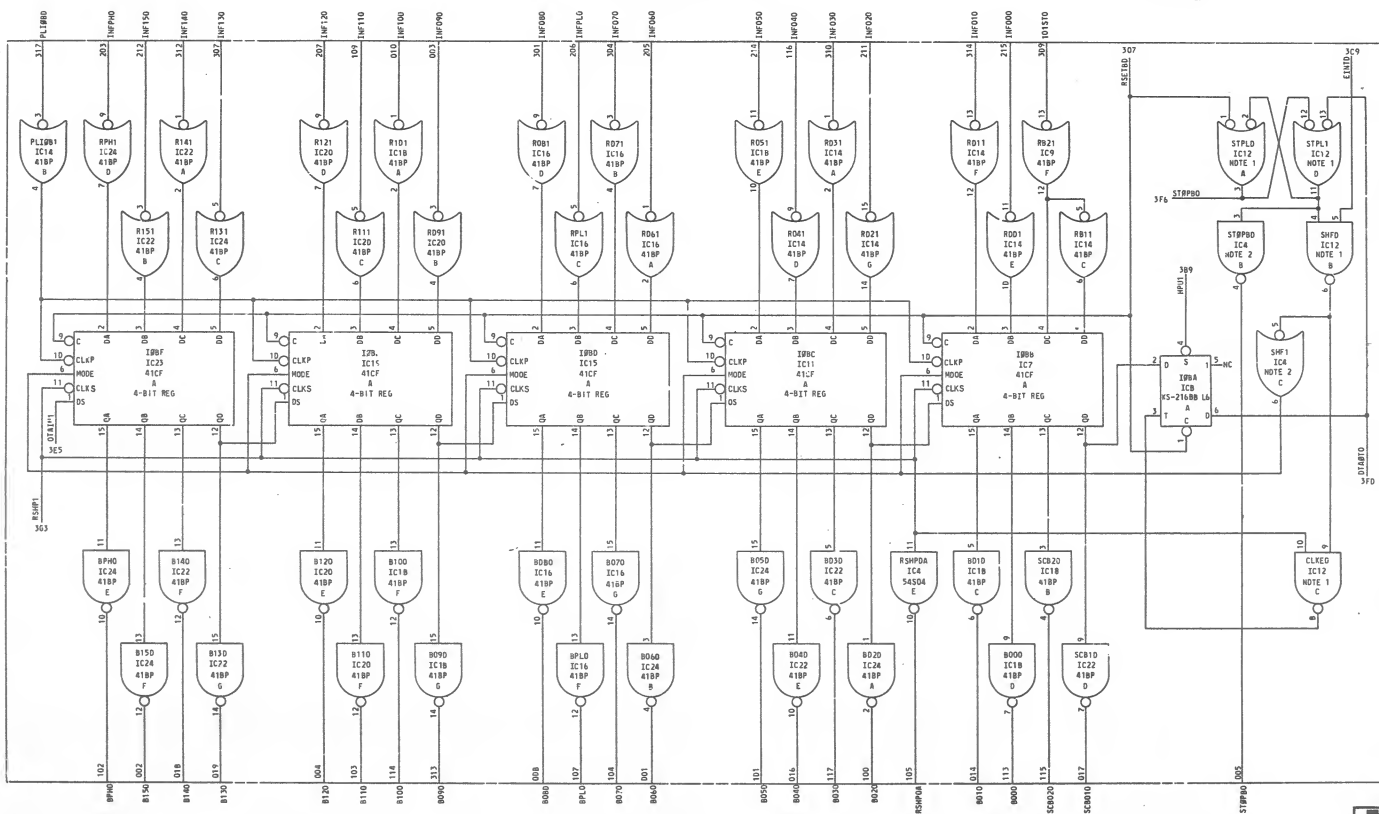
4 SHEETS

BELL TELEPHONE LABORATORIES

65

PART OF CPS JK6 SERIAL PERIPHERAL INTERFACE CIRCUIT

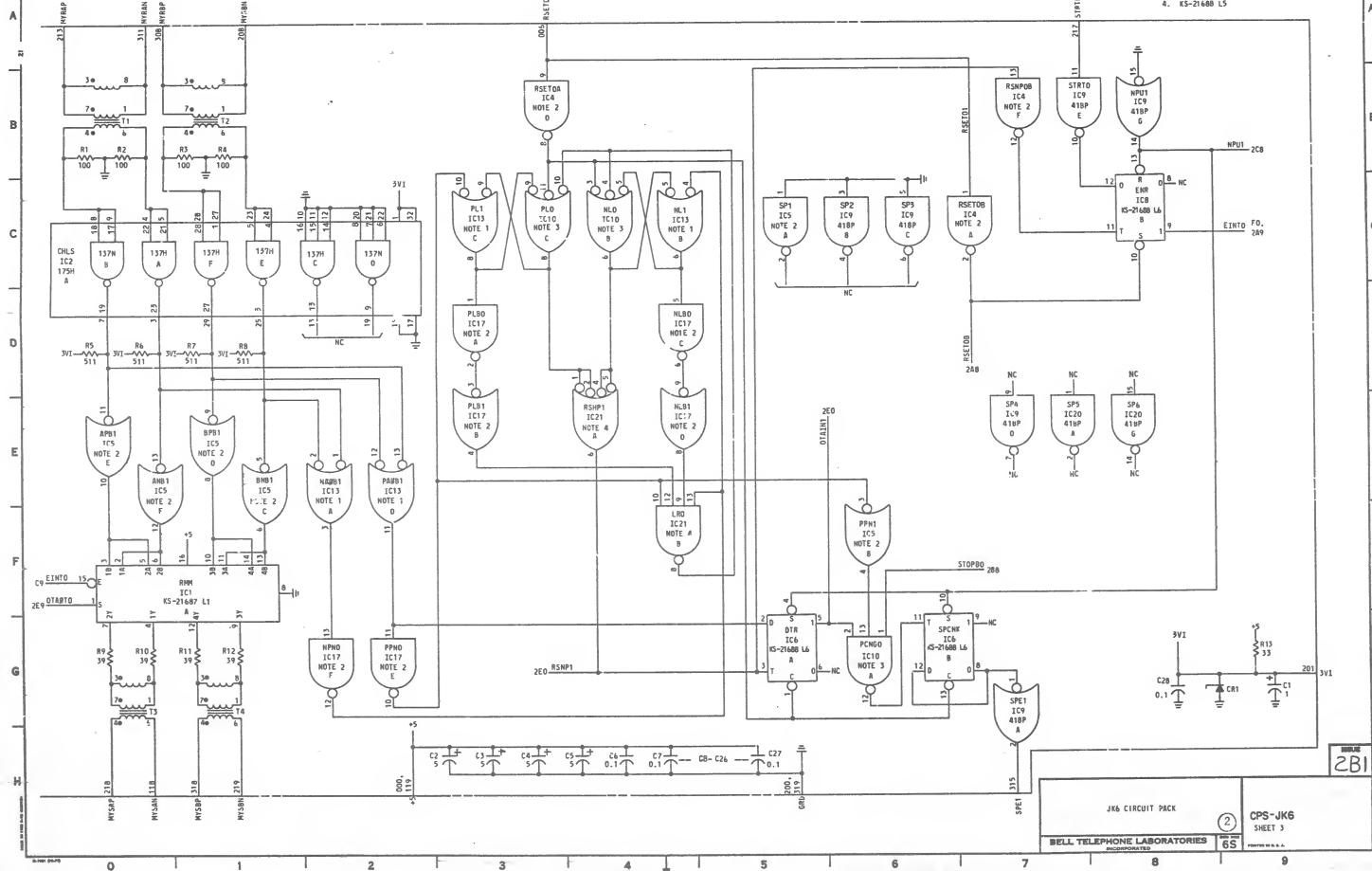
SHEET NOTES:
1. KS-2148B L1
2. KS-2148C L3



PART OF CPS JK6 SERIAL PERIPHERAL INTERFACE B CIRCUIT

SHEET NOTES:

1. K5-21488 L1
2. K5-21488 L3
3. K5-21488 L4
4. K5-21488 L5



PART OF CPS JK6 SERIAL PERIPHERAL INTERFACE & CIRCUIT

COMPONENT LIST INTEGRATED CIRCUIT

LOC CODE	IC1 44698B- KS-21687 L3	IC2 179H	IC4 44694- KS-21688 L3	IC5 44694- KS-21688 L3	IC6 44694- KS-21688 L6	IC7 41CF	IC8 44694- KS-21688 L6	IC9 41BP	IC10 44694- KS-21688 L4	IC11 41CF	IC12 44694- KS-21688 L3	IC13 44694- KS-21688 L3
ELEM ID	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC
A	R9H	3F0	CHLS	3C0	RSET00 3C7	SP1 3C9	UTR 3C5	18B8 207	SP1 3H7	PCHG0 3C6	STPL0 288	NH0B1 3E2
B					STBP00 2C8	PPH1 3F6	SPCK 366		SP2 3C6	NLO 3C4	CHLED 279	HL1 3C4
C					SP1 209	BN1 3E1			SP3 3C6	PLO 3C3		PL1 3C3
D					RSET0A 3B3	BPB1 3E1			STBTD 3B7			PAW1 3E2
E					RSP0A 2F5	APB1 3E0			RS21 227			
F					RSP0A 3B7	ANB1 3E0			HPU1 3B8			

LOC CODE	IC14 41BP	IC15 41CF	IC16 41BP	IC17 44694- KS-21688 L3	IC18 41BP	IC19 41CF	IC20 41BP	IC21 44694- KS-21688 L5	IC22 41BP	IC23 41CF	IC24 41BP
ELEM ID	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC	DESIG SH LOC
A											
B	PL180 286	18B0 2D4	R061 2C4	PLB0 303	R101 282	18B6 232	SP5 3C7	RSPH1 3E4	R161 2D1	18F0 2D1	R020 2F6
C	R071 280		R071 284	PLB1 3E3	SC020 2F7		R091 2C3	L00 3F4	R191 2C1		R040 2-4
D	R011 2C7		RPL1 2C4	NL00 304	B010 277		R111 2C2		R070 2F6		R191 2C1
E	R041 2C5		R081 2D3	NL01 3E4	B000 2F7		R121 2C2		SC010 2F7		RPH1 280
F	R001 2C7		B080 2F4	PPH0 3C2	R051 289		B120 2C2		B040 2F7		BPH0 2C0
G	R071 2D7		BPL0 2F4	NH00 3C2	B100 272		B110 272		B140 2F7		B150 2F1
H	R021 2C6		B070 2F4		B090 2F3		SP6 3C7		B130 2G1		B120 2F5

EXPLANATION

DESIG	CODE
C1	600A,1
(4) C2-C5	601A,5
(2) C6-C8	KS-19774 L5,D,1

DIODE

DESIG	CODE
CR	4469290 KS-21761 L1

RESISTOR

DESIG	CODE
(4) R1-R4	KS-20616 L1A,100
(4) R5-R8	511
(4) R9-R12	39
R13	KS-20616 L1A,33

TRANSFORMER

DESIG	CODE
(4) T1-T4	26446

CIRCUIT DESCRIPTION

THIS PACK CONTAINS A 21-BIT SHIFT REGISTER TO RECEIVE A SERIAL MESSAGE FROM THE JAC. BIPOLAR PULSES ARE RECEIVED FROM EITHER CC VIA THE A OR B INPUT PORTS. CHLS CONVERTS THE RECEIVED PULSES TO TTL LEVELS. THE CLK/PULSE (RSPH1) RECEIVED FROM THE BITSTREAM IS NOMINALLY 75 NSC WIDE. THE RECEIVED DATA (DATAIN) IS HELD STABLE OVER THE TRAILING EDGE OF THE RSPH1 PULSE BY THE DTR F/F.

THE 21-BIT MESSAGE IS CHECKED FOR SINGLE ERRORS BY THE PARITY CHECK F/F (SPCK). A SHIP LATCH IS SET WHEN THE FIRST ONE BIT IS CLOCKED INTO THE DATA F/F. THE SHIFT REGISTER CONTENTS ARE FROZEN BECAUSE THE REGISTER IS SET INTO THE PARALLEL LOAD MODE. 20-BITS OF THE REGISTER ARE AVAILABLE FOR DECODING PURPOSES. THE STATUS OF THE 19 INPUT LEADS ARE LATCHED INTO THE REGISTER AT THE TRAILING EDGE OF A PULSE ON LEAD PLIB00 TO SEND THE 21-BIT MESSAGE BACK TO THE CC THE ENR F/F IS RESET BY A HIGH INPUT ON LEAD STPL1. THE ENR F/F ENABLES THE REPLY MESSAGE AMPLIFIER R9H AND PLACES THE REGISTER INTO THE SERIAL SHIFT MODE. THE DATA APPEARING AT THE OUTPUT OF 18A (STAP00) MODULATES THE TWO CLK/PULSES TO GENERATE BIPOLAR PULSES AT THE A OR B OUTPUT PORTS.

THE CIRCUIT IS INITIALIZED BY A HIGH INPUT ON LEAD RSE01. R13 AND CR1 GENERATE THE 3-VOLT SUPPLY REQUIRED BY THE 175H LEVEL SHIFTERS CHLS.

JK6 CIRCUIT PACK

2

CPS-JK6
SHEET 4

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